REMARKS

The examiner rejected claims 1-23 under 35 U.S.C. 102(b) as being anticipated by Chang et al US Patent 5,634,015.

Claims 1-23 are distinct over Chang. Claim 1, as amended for instance, recites a method that includes... storing a subset of queue descriptors in a cache... receiving a request to perform an enqueue or a dequeue operation with respect to a particular queue; and referencing a corresponding queue descriptor stored in the cache to execute the operations.

As noted by the examiner, Chang's system includes a packet memory (PM), a buffer table entry (BTE), and a generic adapter manager (GAM). In Chang's system packets are stored in the packet memory, and "for each buffer in the packet memory (PM) there is one corresponding buffer table entry" (Col 17, lines 24-26). "In the GAM, packet buffers are linked together through the next buffer pointer in the BTR. Once a packet is stored in the PM, it will be treated as a unit by the GAM 18. To represent this unit, the GAM has one packet table entry (PTE) in its local memory for each existing packet in the PM" (Col. 17, lines 60-63). Thus, Chang stores the queue descriptor for each unit (i.e., queue) in the memory. Chang neither describes nor suggests, "storing a subset of queue descriptors in a cache" as in the applicant's claim 1.

For at least the same reasons, applicant submits claim 1 should be allowed, applicant submits that dependent claims 2-8 should be allowed.

Claim 7 further distinguishes over the Chang. Chang includes a head pointer and a tail pointer as described in col. 18 as follows:

> "A queue has a queue head and a queue tail. A packet can be enqueued either from the queue head (for urgent traffic) or from the queue tail (for synchronous and asynchronous traffic), but a packet can be dequeued only from the queue head. In order to control the packet enqueue and dequeue operations, the GAM 18 has a Queue Control Block (QCB) for every queue defined in the adapter. In every QCB, there is a queue head pointer and a queue tail pointer pointing to the first packet and the last packet in the queue" (Col. 18, lines 6-16).

Chang does not disclose nor suggest using the QCB to modify the queue descriptors. In addition, in col. 33, Chang describes "a step-by-step event sequence from the time a new packet is received at PMI 1 to the time a packet is sent out through PMI 2" (Col. 33, lines 11-12). This description does not include modifying the head pointer or the tail pointer. Hence, the features of returning to memory from the cache potions of the queue descriptor modified be the operation further distinguish claim 7 over the Chang.

Referring to claim 9, claim 9 includes a "memory controller logic that includes a cache to store a subset of the queue descriptors in the memory." Thus, based on these limitations claim 17 is patentable for reasons similar to claim 1.

For at least the same reasons, applicant submits claim 9 should be allowed, applicant submits that dependent claims 10-15 should be allowed.

Referring to claim 16, claim 16 as amended includes a "cache including a subset of all queue descriptors." Thus, based on these limitations claim 16 is patentable for reasons similar to claim 1.

For at least the same reasons, applicant submits claim 16 should be allowed, applicant submits that dependent claims 17-23 should be allowed.

Enclosed is a Petition for Two Month Extension and the required fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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